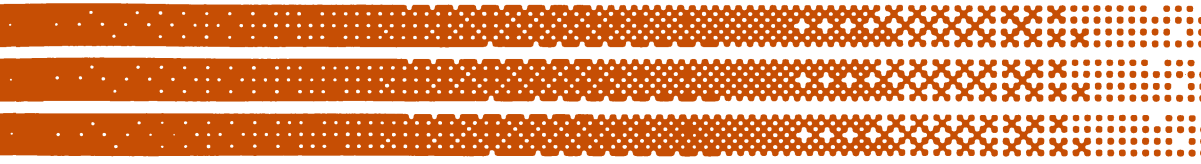


RQDX2 Controller Module

User's Guide

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RQDX2 Controller Module

User's Guide

Prepared by Educational Services
of Digital Equipment Corporation

1st Edition, November 1985

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This user's guide provides information on the configuration, installation, and operation of the RQDX2 disk drive controller module, the associated disks (the RD5n Winchester fixed disk drives and the RX50 diskette drive), and the RQDX1-E and RQDXE extender modules.

Chapter 1, Introduction, provides environmental and functional specifications for the RQDX2 controller module, the RD5n fixed disk drive, the RX50 diskette drive, and the RQDX1-E and RQDXE extender module options.

Chapter 2, Functional Description, gives a functional description of the RQDX2 controller module.

Chapter 3, Configuration and Installation, presents configuration and installation information for the RQDX2 controller module and the RQDX1-E and RQDXE extender module options.

Chapter 4, Registers and Commands, describes the programmable registers that are LSI-11 bus addressable on the RQDX2 controller module. Mass Storage Control Protocol (MSCP) and Diagnostics and Utilities Protocol (DUP) are summarized.

Chapter 5, Diagnostics, provides diagnostic testing and error detection information.

Appendix A gives the RQDX2 controller module backplane pin assignments.

Appendix B gives the RQDX2 controller module cable signals.

Appendix C gives the disk drive cable connector pin assignments.

The RQDX2 Field Maintenance Print Set (MP-01731-01) and UDA50 Programmer's Documentation Kit (QP-905-GZ) provide additional information and may be of interest to RQDX2 controller module users.

In addition, users may refer to documentation for the system in which the RQDX2 controller module is installed.

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DESCRIPTION

The RQDX2 disk drive controller module interfaces the RD51/RD52/RD53 (RD5n) fixed disk drives and/or the RX50 diskette drive to any quad- or hex-size backplane that uses a 16-, 18-, or 22-bit LSI-11 bus. The backplane must be in a mounting box (such as a BA23 enclosure) that provides a control panel and a signal distribution panel. A single RQDX2 module controls any one of the configurations listed in Table 1-1.

Table 1-1 RQDX2 Controller Module Configurations

Configuration	Physical Disk Drives	Logical Disk Drive Numbers
1	One RD5n One RX50	Unit 0 = RD5n Unit 1, 2 = RX50
2	Two RX50s	Unit 0, 1 = RX50 Unit 2, 3 = RX50
3*	Two RD5n(s) One RX50	Unit 0 = RD5n Unit 1 = RD5n Unit 2, 3 = RX50
4*	Two RD5n(s)	Unit 0 = RD5n Unit 1 = RD5n
5	One RX50	Unit 0, 1 = RX50
6	One RD5n	Unit 0 = RD5n

* These configurations require the use of the optional RQDXE extender module. See Chapter 3 for more RQDXE information.

The RD51, RD52, and RD53 disk drives are random access storage devices. All drives use two nonremovable 133.4 mm (5.25 in) disks as storage media. The total formatted storage capacity of the RD51 drive is 11 Mbytes, the RD52 drive is 31 Mbytes, and the RD53 drive is 71 Mbytes.

The RX50 diskette drive is a random access storage device that uses two single-sided 133.4 mm (5.25 in) RX50K diskettes. The total storage capacity of the RX50 diskette drive is 800 Kbytes of formatted data.

The RQDXE extender module option provides cable connection to a disk(s) or diskette(s) that is mounted externally from a mounting box.

FEATURES

The RQDX2 controller module has the following features.

- Single quad-size module
- Supports DMA data transfers in 16-, 18-, or 22-bit addressing modes
- Supports block mode transfers with MSV11-P memories
- Supports 22-bit addressing on an LSI-11 bus
- Memory parity error abort feature for use with memories that have a parity option
- Requires no jumper/switch reconfiguration when adding or removing RD5n or RX50 drives

RQDX2 DISK CONTROLLER MODULE SPECIFICATIONS

This listing presents physical and operational specifications regarding the RQDX2 module while Table 1-2 describes the environmental specifications.

Module	1 quad-size module, M8639-YB
Size	Height: 26.56 cm (10.46 in) Width: 1.27 cm (0.5 in) Length: 22.70 cm (8.94 in)
Power requirements	+5 Vdc +5% at 6.4 A (typ.) 8.0 A (max.) +12 Vdc +5% at 60 mA (typ.) 100 mA (max.)
Bus loads	
AC	2.5
DC	1
Addressing modes	16-, 18-, and 22-bit (determined by user)

Limitations	The RQDX2 module will not fit in the dual-height LSI-11 miniseries H9281 backplane.	
	KDF11-BF or later RT-11 V5.2 or later Micro/RSX V1.1 or later RSX-11M-PLUS V2.1, update E or later RSX-11M V4.1, update E or later RSTS/E V9.0 or later Micro/RSTS V2.0 or later	
Drives per controller	Up to four logical units	
LSI-11 bus-addressable registers	2	
Base device address (standard)	Addressing mode	Address (octal)
	16-bit	172150
	18-bit	772150
	22-bit	17772150
Vector	Software selectable (Normally set at 154)	
DMA data transfer rate	800 ns/word (peak) controller to host 250 K bits/s RX50 drive to controller 5 M bits/s RD5n drive to controller 35 K bytes/s RX50 drive to host 160 K bytes/s RD5n drive to host	
Airflow	Operating up to 50°C Maximum temperature rise across module must not exceed 20°C (68°F) input to output	

Table 1-2 Environmental Specifications for the RQDX3 Module

Environment	Operating	Nonoperating
Temperature range	5°C--50°C (41°F--122°F)	-40°C--66°C (-40°F--150°F)
Relative humidity (noncondensing)	10% to 95%	10% to 95%
Maximum altitude	2.4 km (8,000 ft)	9.1 km (30,000 ft)

RQDXE EXTENDER MODULE SPECIFICATIONS

This listing presents physical and operational specifications regarding the RQDXE module while Table 1-3 describes the environmental specifications.

Module 1 dual-size module, M7513

Size Height: 13.2 cm (5.2 in)
 Width: 1.27 cm (0.5 in)
 Length: 22.8 cm (8.9 in)

Power requirements +5 Vdc at 0.8 A (typ.) 0.9 A (max.)

Bus Loads

AC bus 0
DC bus 1

Airflow

Operating up to 50°C Maximum temperature rise across module
 must not exceed 20°C (68°F) input to
 output

Table 1-3 Environmental Specifications for the RQDXE Module

Environment	Operating	Nonoperating
Temperature range	5°C--60°C (41°F--140°F)	-40°C--66°C (-40°F--150°F)
Relative Humidity (noncondensing)	10% to 95%	10% to 95%
Maximum altitude	2.4 km (8,000 ft)	9.1 km (30,000 ft)

INTRODUCTION

The RQDX2 controller module interfaces the RD5n disk drive(s) and/or RX50 diskette drive(s) to a 16-, 18-, or 22-bit LSI-11 bus. One RQDX2 controller module can support up to four logical units in combinations of RD5n and RX50 drives (up to two RD5n drives per RQDX2 controller module). See Table 1-1. The RQDX2 controller module (M8639-YB) contains the necessary LSI-11 bus transceivers and decoders, programmable registers, controller timing and sequence logic, and data formatting circuits to read and write on the RD5n disk media and/or the RX50 diskette media.

BLOCK DIAGRAM DESCRIPTION

Figure 2-1 shows the main functional subsections of the RQDX2 module. This block diagram illustrates the basic architecture and the data path relationships of the major subsections. The RQDX2 controller module is a bus-oriented system controlled by a system control function shared by the T-11 chip and the main high-speed controller.

The major subsections of the RQDX2 are as follows.

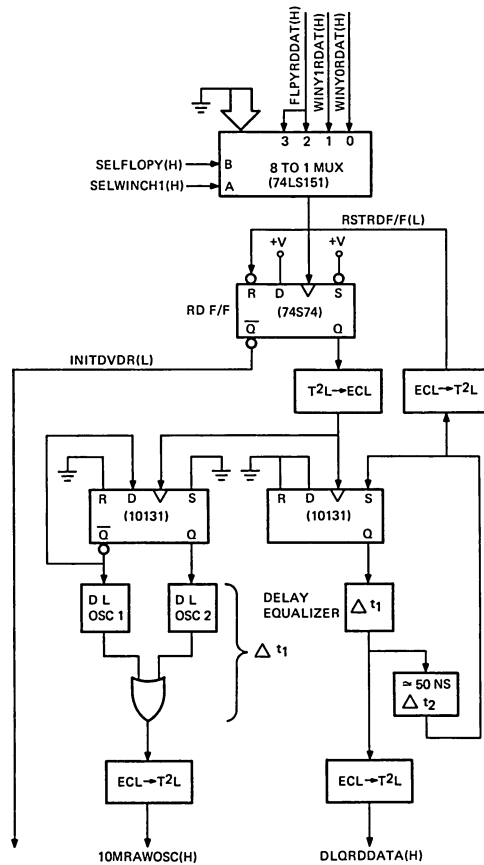
- Shuffle step oscillator
- Phase-locked loop
- Data recovery
- Sync mark detector
- Serializer/deserializer
- Modified Frequency Modulation (MFM) encoder/precomp generator
- Interrupt vector register
- SA read/write registers, IP register
- Q-Bus transceivers and handshake controllers
- RQDX2 control logic: T-11 chip and main high-speed controller
- Memory address counter/register
- 8 K X 16 RAM
- Disk drive control register and status buffer
- T-11 RAM address pointer and Arithmetic Logic Unit (ALU)
- Bidirectional byte multiplexer
- 16 K X 16 EPROM
- Q-Bus DMA pointer and ALU



Figure 2-1 RQDX2 Controller Module Functional Block Diagram

SHUFFLE STEP OSCILLATOR

The shuffle step oscillator (Figure 2-2) is a system of two matched 10 MHz oscillators, a small asynchronous oscillator controller, and a read data delay equalizer. When one of the oscillators is generating a raw read clock signal for the phase-locked loop (PLL), the other oscillator is in standby. At each raw read data pulse, the system commands the active oscillator to turn off and the standby oscillator to become active. This causes the oscillators to shuffle to keep in step with the RAW read data. The read data delay equalizer section delays the RAW read data to compensate for the short amount of time that it takes to shuffle the oscillators.

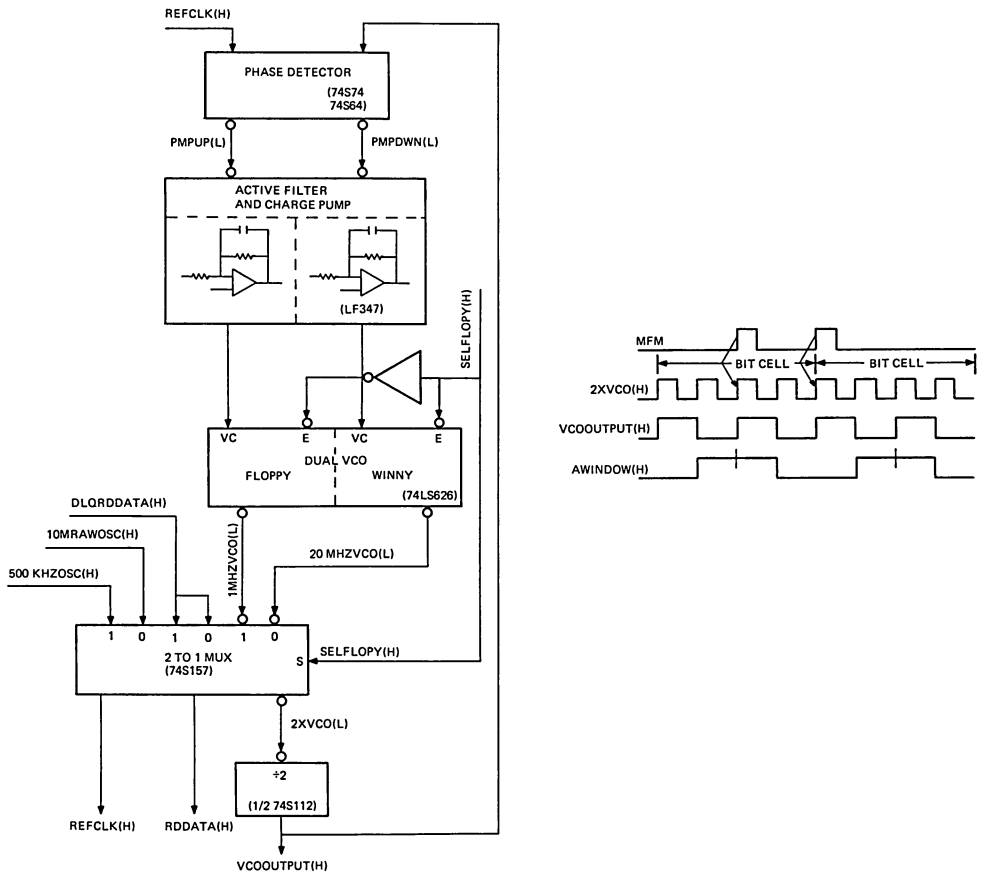


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Figure 2-2 Shuffle Step Oscillator

PHASE-LOCKED LOOP

Figure 2-3 shows the Phase-Locked Loop (PLL) logic. The PLL is a dual-channel, single-mode system. Dual channel provides one channel for the RX50 diskette drive(s) and one channel for the RD5n disk drive(s). The function of the PLL logic is to provide the flywheel effect for the shuffle step oscillator output, thus integrating the effects of the pulse drift in the raw read data. The system feeds the output of the PLL into a counter that generates two data recovery window signals. These windows center the read data pulses. (At any given time, one of these windows will frame the data.) The sync mark detector selects the proper data framing window automatically.

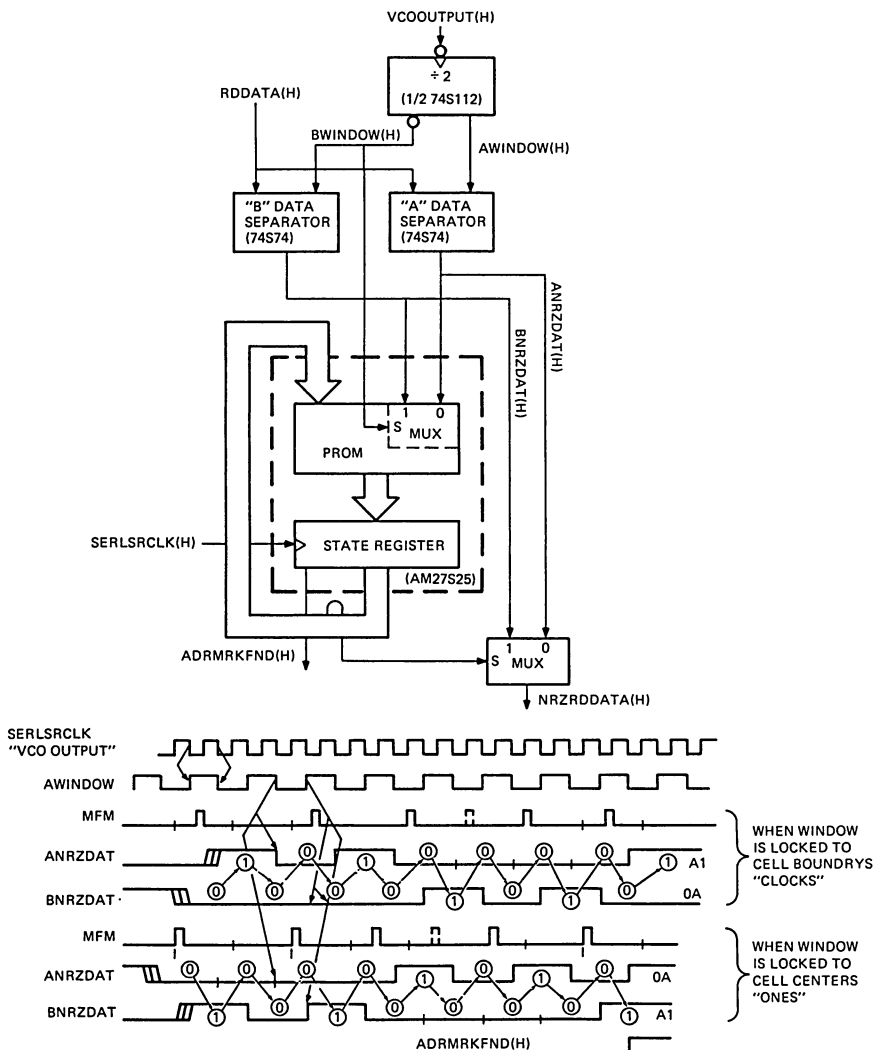


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Figure 2-3 Phase-Locked Loop Logic

DATA RECOVERY

The data recovery logic (Figure 2-4) consists of two single-bit, edge-triggered, double-buffered registers. The registers are cross-coupled to capture the read data occurring anywhere within either data framing window. Together with the phase locked loop output, the data recovery logic produces an NRZ read data stream.



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Figure 2-4 Data Recovery and Sync Mark Detector Logic

SYNC MARK DETECTOR

The sync mark detector logic (Figure 2-4) provides two functions. One, it detects the sync mark, and two, it selects the proper stream from the data recovery logic. The system analyses both data recovery bit streams to find the sync mark. Upon detection of the sync mark in either stream, the serializer/deserializer logic receives the desired data stream.

SERIALIZER/DESERIALIZER

Figure 2-5 shows the serializer/deserializer. The serializer/deserializer consists of the following four parts.

- A double-buffered serial in/parallel out register
- A double-buffered parallel in/serial out register
- A CRC generator/checker
- A high-speed finite state machine controller

The Serial In/Parallel Out (SIPO) logic shifts the serial read data through the CRC generator and forms an 8-bit parallel byte. The byte is buffered for data transfer.

The Parallel In/Serial Out (PISO) logic receives the parallel write data, buffers it, and shifts this data serially through the CRC generator to the MFM encoder and precomp generator. This serial data becomes the write data that is sent to the disk.

The high-speed machine controller controls both the SIPO and PISO logic.

MFM ENCODER/PRECOMP GENERATOR

The Modified Frequency Modulation (MFM) encoder/precomp generator logic (Figure 2-5) receives the serial data that is written to the disk and performs the following operations.

1. It generates an MFM data bit stream.
2. It precompensates the MFM bit stream (for both the RD5n disk drive and the RX50 diskette drive devices).
3. It generates the sync mark bit sequence on command.



**Figure 2-5 Serializer/Deserializer and MFM Encoder/Precomp
Generator Logic**

INTERRUPT VECTOR REGISTER

During an interrupt sequence, the system gates the contents of the interrupt vector register (Figure 2-6) to the Q-Bus for use as the vector. The MSCP initialization function supplies the T-11 chip on the RQDX2 controller module with the vector number. The T-11 chip loads this number into the interrupt vector register.

SA READ REGISTER, SA WRITE REGISTER, IP REGISTER

Figure 2-6 shows the Status and Address registers (SA). The T-11 chip and the Q-Bus processor use these registers for the MSCP port initialization sequence. Both SA registers occupy the same Q-Bus I/O page address.

The SA read register is written into by the T-11 chip and read from by the host Q-Bus processor. The system uses this register to pass initialization status to the Q-Bus processor.

The SA write register is written into by the Q-Bus processor and read from by the T-11 chip. The system uses this register during the initial sequence to pass the MSCP command buffer address and interrupt vector to the T-11 chip.

The system uses the IP register to begin the initialization sequence when this register is written into by the Q-Bus processor. When the host Q-Bus processor reads from the IP register, the RQDX2 controller module initiates a polling routine.

Q-BUS TRANSCEIVERS AND HANDSHAKE CONTROLLERS

The RQDX2 controller module interfaces to the Q-Bus through Q-Bus drivers, Q-Bus receivers, and control circuits. Figure 2-6 shows the control circuits. These circuits provide the handshake signals necessary to interrupt the Q-Bus, obtain control of the Q-Bus for DMA, and interface the programmed SA and IP registers to the Q-Bus.

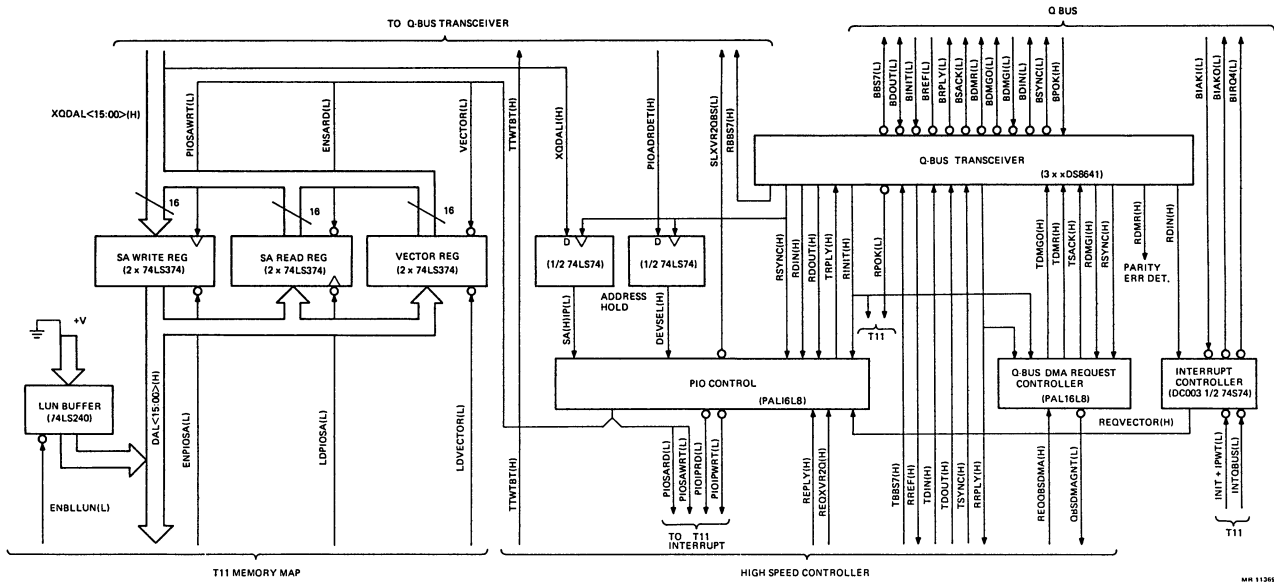


Figure 2-6 Interrupt Vector Register, SA Register, and Q-Bus Interface Logic

RQDX2 CONTROL LOGIC

The T-11 chip and the main high-speed controller share the supervisory control of the complete RQDX2 controller module. These two devices share the internal data address bus (DAL bus). Refer to Figure 2-1.

The T-11 chip controls all housekeeping functions considered to be slow or those that require data processing. The T-11 chip is configured into the 16-bit static mode driven by a 7.5 MHz clock. Figure 2-7 shows the T-11 logic, along with the RAM and ROM logic.

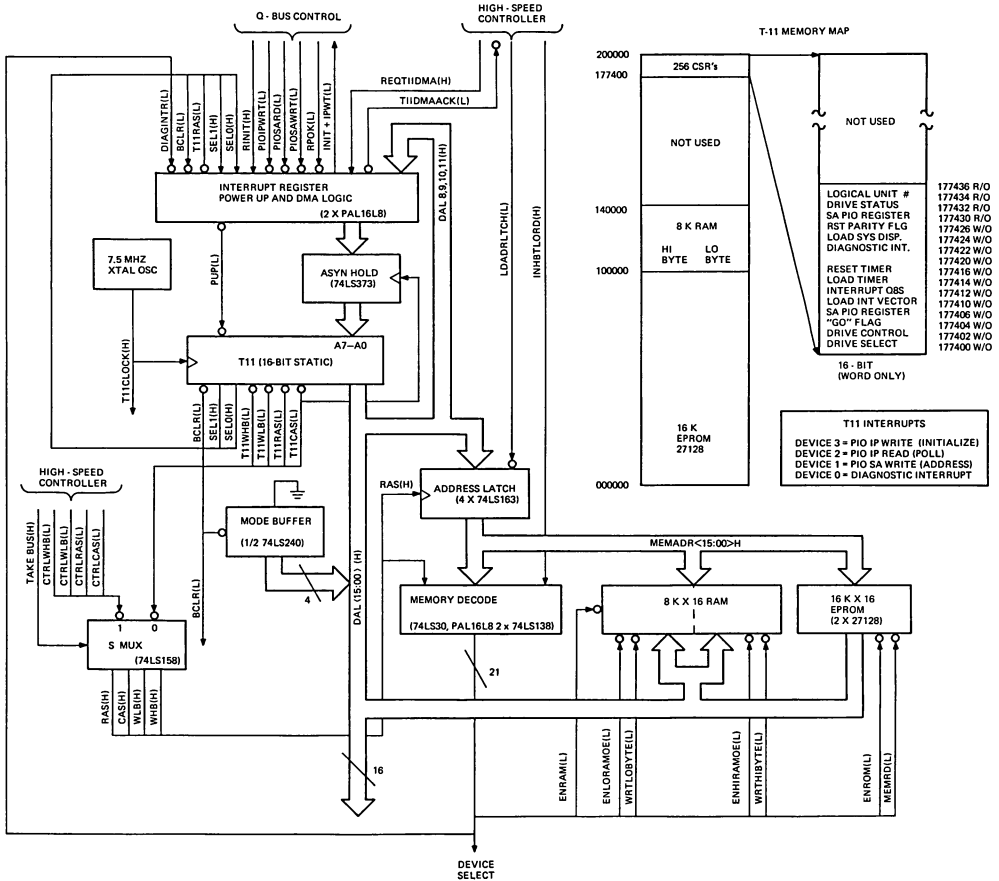


Figure 2-7 T-11, RAM and ROM Logic

The T-11 chip sets up all disk drive control signals, initializes the timer, clears the parity error flag, and resets the shuffle step oscillator. The T-11 chip then sets up the Device Control Block (DCB) with parameters for the high-speed controller, initializes the response word with 1s, and then sets the GO flag in the I/O map. The high-speed controller, upon receipt of the GO signal, requests direct memory access to the DAL bus from the T-11 chip. Upon receipt of the T11DMAACK signal, the controller takes control of the DAL bus and begins the operation specified in the function code. Upon completion, the system places various parameters in T-11 RAM, fills in the controller response word (in the DCB), clears the GO bit, and returns control to the T-11 chip. The system must complete all high-speed controller operations within one second or the timer logic will terminate controller operation.

MEMORY ADDRESS COUNTER/REGISTER

Figure 2-7 shows the memory address counter/register that the system uses to latch the T-11 memory address during the address phase of the bus cycle. The high-speed controller uses the counter function of the address register to form a RAM pointer that the system can increment.

8 K X 16 RAM

As Figure 2-7 shows, the 8 K X 16 RAM is divided into the following three major sections.

- T-11 work space
- Device control block
- Sector buffer

DISK DRIVE CONTROL REGISTER AND STATUS BUFFER

Figure 2-9 shows the disk drive control register and status buffer. Under T-11 control, the disk drive control register provides drive selection and head control, including cylinder seeks on the selected drive. This register also contains static control information for the PLL and serializer. The drive status buffer interfaces the selected drive status to the DAL bus so that it can be interrogated by either the T-11 chip or the high-speed controller.

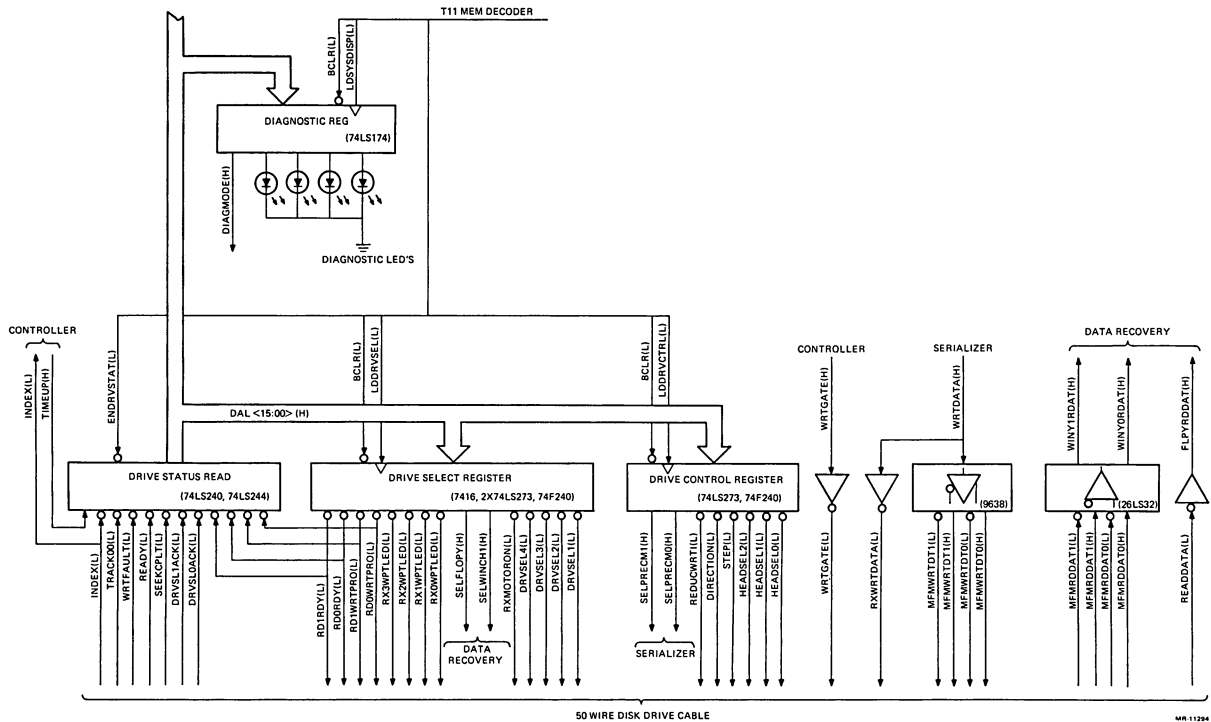


Figure 2-9 Disk Drive Control Register and Status Buffer

T-11 RAM ADDRESS POINTER AND ALU

The T-11 RAM pointer logic consists of an address counter and an ALU. The high-speed controller logic loads the beginning and ending T-11 RAM addresses into the registers within the address counter. The controller then uses these pointers to specify the locations in the T-11 RAM where the system is to transfer data during Q-Bus DMA and disk data transfers. The high-speed controller increments the pointers and monitors the ALU to determine when it reaches the ending address.

BIDIRECTIONAL BYTE MULTIPLEXER

The system uses the bidirectional byte multiplexer to interface the 8-bit input/output of the serializer/deserializer to the 16-bit RAM via the DAL bus.

During the read operation, the byte multiplexer causes the 8-bit byte from the serializer/deserializer to appear on both high and low bytes of the 16-bit DAL bus. The high-speed controller can then selectively write the byte into either the high or low byte section of the 8 K X 16 RAM.

During a write operation, the system can use the bidirectional byte multiplexer, again under control of the high-speed controller, to place the high byte into the low byte position of the DAL bus. The system disables the low byte output of the RAM at this time.

16 K X 16 EPROM

The system uses the 16 K X 16 EPROM to store the T-11 instructions. In addition, the EPROM also stores the disk drive characteristics and RQDX2 self-test codes. Support for new disk drives may require EPROM updates.

Q-BUS DMA POINTER AND ALU

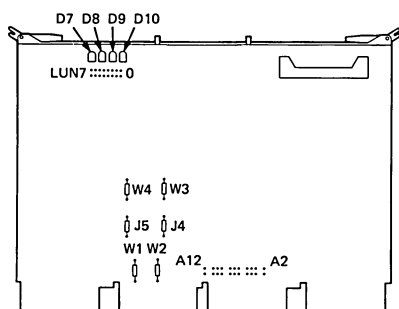
The Q-Bus DMA pointer logic consists of an address counter and an ALU. The high-speed controller controls this logic and uses it to hold the Q-Bus address during a DMA process.

The high-speed controller also uses this logic as a byte comparator to perform sector seek functions during read/write operations.

INTRODUCTION

The RQDX2 controller module has two jumper groupings for module configuring the MicroPDP-11 system: one for the CSR address and the other for the logical unit number. In addition, the RQDX1-E and RQDXE extender modules have jumpers for configuration to support various combinations of RD5n and RX50 disk drives in a system.

You can install the RQDX2 controller module in any unoccupied backplane slot. The RQDX1-E and RQDXE extender modules should reside in the backplane slot immediately following the RQDX2 controller module.



NOTES:

1. ADDRESS SELECTION (A12 THROUGH A2) AND LOGICAL UNIT NUMBER SELECTION (LUN7 THROUGH LUN0) IS MADE BY ATTACHING TWO POSITION JUMPER CLIPS (PART NO. 12-18783-00). THIS ELIMINATES THE NEED TO WIRE WRAP JUMPERS ONTO THE ADDRESS OR LOGICAL UNIT NUMBER STAKES.
2. JUMPERS W1 AND W2 ARE IN FOR Q/Q AND Q22/Q22 SLOTS ARE OUT FOR Q/CD AND Q22/CD SLOTS PROVIDE GRANT CONTINUITY
3. JUMPERS W3, W4, J4 AND J5 ARE RESERVED FOR MANUFACTURE TESTING PURPOSES ONLY.

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Figure 3-1 RQDX2 Controller Module Jumper Locations

RQDX2 CONFIGURATION

Module jumpers A2 through A12 configure the CSR address, and jumpers LUN 1 through LUN 7 configure the logical unit number (for the MicroPDP-11). These jumpers are two-position clips (part number 12-18783-00) that eliminate the need for wire-wrapping.

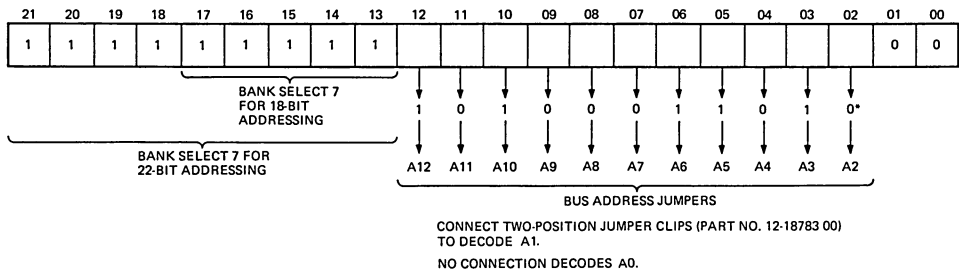
CSR Address

Figure 3-1 shows the location of the RQDX2 controller module CSR address jumpers, A2 through A12. The first RQDX2 installed has a fixed CSR address of 772150 that is factory configured. Table 3-1 gives the factory configuration.

If you install a second RQDX2 or MSCP device in the system, you must not configure the CSR address to the factory address. Configure it according to system address space requirements. Figure 3-2 shows the general format for configuring the CSR address.

Table 3-1 RQDX2 CSR Address Jumper Factory Configuration

Jumper	State
A2	Out
A3	In
A4	Out
A5	In
A6	In
A7	Out
A8	Out
A9	Out
A10	In
A11	Out
A12	In



*FACTORY
CONFIGURATION

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Figure 3-2 RQDX2 CSR Address Jumper Format

Logical Unit Number

Figure 3-1 shows the location of the RQDX2 controller module Logical Unit Number (LUN) jumpers, LUN0 through LUN5. They represent a binary coded value and are used for configuring the MicroPDP-11 system. When used in MicroVAX systems, the LUN jumpers are not on the RQDX2 module. The highest LUN allowable is 255. However, the number of actual physical units in a system is normally less than 35. Therefore, LUN6 and LUN7 are not normally jumpered.

Jumpers LUN0 through LUN5 are configured for the lowest logical unit number assigned to any disk/diskette drive controlled by the module. The controller automatically sizes the logical unit configuration during initialization to determine how many of up to four possible units are actually connected. This eliminates the need for jumper reconfiguration when you add or remove drive units (RD5n or RX50 drives) from the module's control. Table 3-2 gives the LUN jumper factory configuration. Table 3-3 lists several examples of the LUN (or binary coded value) jumper placement.

Table 3-2 RQDX2 LUN Jumper Factory Ship Configuration

Jumper	State	
LUN0	Out	Logical unit number (0)*
LUN1	Out	
LUN2	Out	
LUN3	Out	
LUN4	Out	
LUN5	Out	
LUN6	Out	
LUN7	Out	

* Indicates that LUNs 0--3 are assigned to this controller module. Controller automatically determines how many physical units, between 1 and 4, are present.

Table 3-3 RQDX2 Logical Unit Number (LUN) Jumper Format

LUN Jumper BCD	7	6	5	4	3	2	1	0
	128	64	32	16	8	4	2	1
Drives 0-3	Out	Out	Out	Out	Out	Out	Out	Out
Drives 4-7	Out	Out	Out	Out	Out	In	Out	Out
Drives 8-11	Out	Out	Out	Out	In	Out	Out	Out
o								
o								
o								
Drives 32-35	Out	Out	In	Out	Out	Out	Out	Out

Interrupt Vector

The interrupt vector has a range of 0 to 774 and is software selectable. (A vector selected by software must be greater than 0.) The RQDX2 controller module typically uses interrupt vector 154.

Interrupt Request Level

The RQDX2 controller module interrupts at priority level 4 determined by the DC003 chip.

RQDX2 INSTALLATION

You usually install the RQDX2 controller module in the last unoccupied slot of the backplane. If you leave empty slots between the other modules and the controller module, install grant cards (part number G7272) in those empty slots to accommodate the interrupt and direct memory access structure of the backplane.

Before installing the module, make sure that the CSR address and LUN jumpers are properly configured.

System Cable Installation

You install the 50-conductor signal cable (part number BC02D-1D) to the J1 connector on the controller module. You must connect this cable to a signal distribution panel that will connect the appropriate signals to the RD5n and/or RX50 drives. Figure 3-3 shows an example of the MicroPDP-11 signal distribution panel connecting the controller module to an RD5n disk drive and an RX50 diskette drive. The RD5n disk drive requires two signal cable connections: a 20-conductor cable (part number 17-00282-00) and a 34-conductor cable (part number 17-00286-00). The RX50 diskette drive requires a single 34-conductor signal cable (part number 17-00285-02).

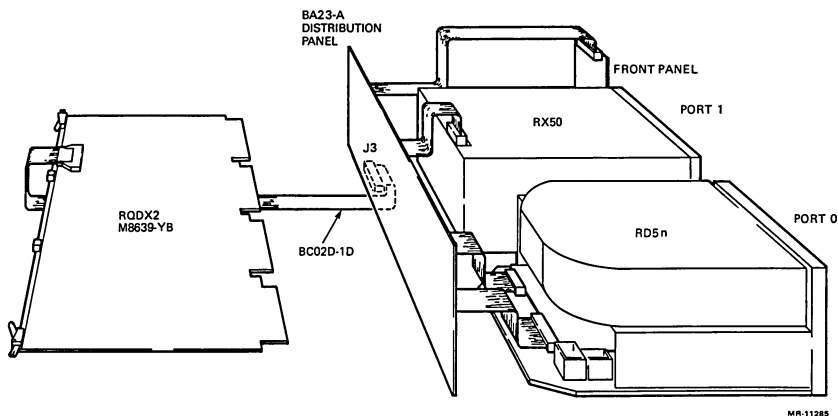


Figure 3-3 RQDX2 Typical System Cable Installation

RQDX1-E AND RQDXE EXTENDER MODULE OPTIONS

The RQDX1-E (M7512) and RQDXE (M7513) are dual-height modules supporting the RQDX2 controller module in several systems. Typically in the MicroPDP-11 system, you house the RQDX2 controller module in the same mounting box as the disk and/or diskette drives that it controls. However, if the system mounting box cannot accommodate all of these drives, you must use the optional extender modules to connect the controller module signals to the externally housed disk drive(s).

The main difference between the M7512 and M7513 modules is that the M7512 module supports one external disk drive in addition to the internal drive(s) and the M7513 module supports a maximum of four external drives. In addition, you can repower any external desktop subsystem (RD5n-D) drives connected to the RQDXE without rebooting the system.

RQDX1-E Module Configuration

The M7512 extender module has jumpers for configuring an external disk drive to the RQDX2 controller module. Figure 3-4 shows the jumper locations, and Figure 3-5 shows jumper placement for both RD5n and RX50 drive installations.

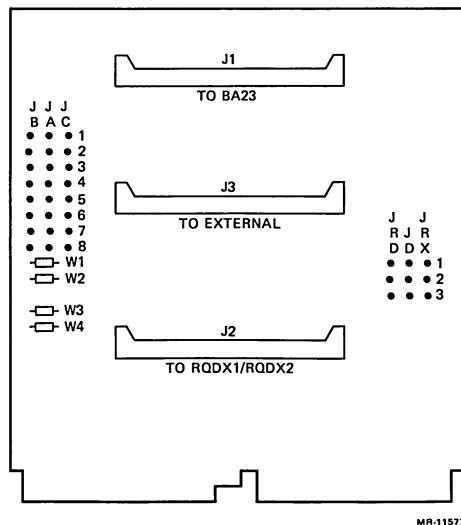


Figure 3-4 RQDX1-E Extender Module Jumper Locations

DESCRIPTION	JUMPER			RD5n*	RX50
FACTORY SET DO NOT CHANGE	JRD1	JD1	JRX1	 O	 O
	JRD2	JD2	JRX2	 O	 O
	JRD3	JD3	JRX3	O O O	O O O
READ/WRITE	JB1	JA1	JC1	 O	 O
	JB2	JA2	JC2	 O	 O
	JB3	JA3	JC3	 O	 O
	JB4	JA4	JC4	 O	 O
	JB5	JA5	JC5	 O	 O
	JB6	JA6	JC6	 O	 O
	JB7	JA7	JC7	 O	 O
	JB8	JA8	JC8	O O O	O O O

* FACTORY CONFIGURATION.

NOTE: O O OR O JUMPER NOT INSTALLED
O

 OR  JUMPER INSTALLED

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Figure 3-5 RQDX1-E Jumper Placement

RQDXE Module Configuration

Figure 3-6 shows the RQDXE extender module jumper locations. Columns A--E of Figure 3-7 identify five possible combinations of drives internal to a BA23-A system enclosure. Columns A--L of Figure 3-8 identify 12 possible combinations of drives external to a BA23-A system enclosure. Some combinations are not possible because the BA23-A system enclosure lacks the necessary front panel controls and power supply capacity to support two Winchester drives. The RQDXE is not supported in the BA123 system enclosure.

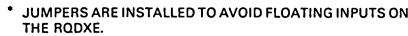
The terms "Port 0" and "Port 1" in Figures 3-7 and 3-8 indicate the physical position of the drive in a BA23-A system or BA23-C expansion box. Refer to Figure 3-3.

Disks contained in desktop or rack mount enclosures use the same terms. In a desktop or rack mount enclosure, connector J1 is Port 0 and connector J2 is Port 1.

The terms RD0, RD1, RD2, and RD3 in Figures 3-7 and 3-8 are Winchester drive number designations that determine how the system software will identify the drive (e.g. RD0 = DUA0 for a system running MicroVMS).

To configure the RQDXE module to meet your system requirements, use the following procedure.

1. Install jumpers in accordance with Figure 3-7. This determines the configuration of the disks in the BA23-A system enclosure. Column C is a typical configuration.



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- A drive number designation cannot be selected twice. For example if the BA23-A system enclosure contains RDO in Port 0 and a second Winchester is added in a BA23-C expansion enclosure it must be designated RD1.

		A	B	C	D	E	F	G	H	I	J	K	L
PORT 0	RD0	X	X	X	-	-	-	-	-	-	-	-	-
	RD1	-	-	-	X	X	X	-	-	-	-	-	-
	RD2	-	-	-	-	-	-	X	X	X	X	-	-
	RD3	-	-	-	-	-	-	-	-	-	-	X	-
PORT 1	RD0	-	-	-	-	X	-	-	-	-	-	-	-
	RD1	-	X	-	-	-	-	-	-	X	-	-	-
	RD2	-	-	-	-	-	X	-	-	-	-	X	-
	RD3	-	-	-	-	-	-	-	-	-	X	-	-
	RX50	-	-	X	-	-	-	X	-	-	-	-	X
RDY AND WRT PROT	A1 A2												
	A3 A4												
	B1 B2												
	B3 B4												
	C1 C2												
	C3 C4												
	D1 D2												
	D3 D4												
DRV SEL	E1 E2												
	E3 E4												
	F1 F2												
	F3 F4												
	H1 H2												
	H3 H4												
DRV ACK	K1 K2												
	K3 K4												
EX PORT SEL	L1												
	L3 L4												
	M1 M2												
	M4												

NOTES

1. COLUMN D REPRESENTS THE FACTORY CONFIGURATION.
2. CONFIGURATIONS B, E, F, H, I, J, K, AND L ARE NOT SUPPORTED AT THIS TIME. THEY ARE USED FOR REFERENCE ONLY.

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Figure 3-8 RQDXE Placement for the BA23-C Enclosure

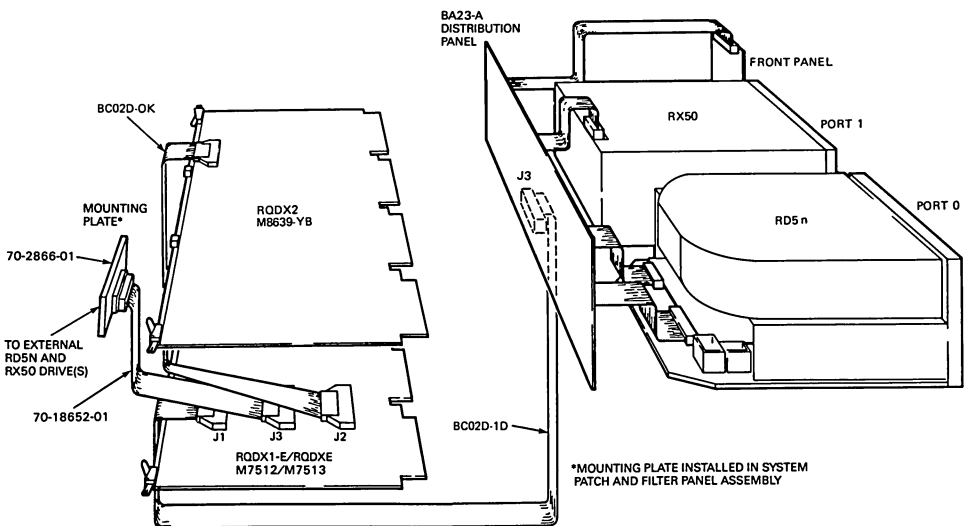
RQDX1-E and RQDXE INSTALLATION

You install the M7512 and M7513 dual-height modules in connectors A and B in the backplane slot directly below the controller module. Connector J2 receives signals from the RQDX2 controller module. The other connectors (J1 and J3) distribute these signals to the externally housed disk and diskette drives. Prior to installing either extender module in a backplane, check the jumper configuration.

System Cable Installation

Figure 3-9 shows the installation of either an RQDX2-E or RQDXE extender module in a typical system configuration, the BA23 mounting box. A cable (part number BC02D-0K) connects the RQDX2 controller module to either extender module through the J2 connector.

Another cable (part number 70-18652-01) attached to the J3 connector connects the extender module to a mounting plate (part number 74-2866-01) that is mounted to the system's patch and filter panel assembly. (You can order the entire cable and mounting plate assembly using part number 70-20691-01.) This external plate provides the signals sent to the external drive. A third cable (part number BC02D-1D) that is attached to the J1 connector on the RQDX1-E extender module is connected to the signal distribution panel in the mounting box, providing signals to the disk or diskette drive(s) installed in the system mounting box.



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Figure 3-9 RQDX1-E and RQDXE Typical System Cable Installation

DISK DRIVES

You use the RQDX2 controller and the extender modules to connect the RD51/52/53 disk drives into the extended LSI-11 bus. Each system technical manual includes the RD51/52/53 specifications and configuration and installation details. The disk drive subsystem manual includes additional disk drive details.

INTRODUCTION

The RQDX2 controller module contains two registers that a Q-Bus address can access. A number of other registers reside on the module, but these are accessible only to the T-11 logic within the module.

The module uses mass storage control protocol (MSCP) to communicate with the host Q-Bus processor. Detailed information regarding MSCP is available in the UDA50 Programmer's Documentation Kit (QP-905-GZ).

REGISTERS

The programmable registers on the RQDX2 controller module are the Initialize and Poll register (IP) and the Status and Address registers (SA). The system can address these registers like any memory location.

Initialize and Poll Register (IP)

The host begins the initialization sequence either by issuing a bus initialize or using the IP initialize operation. The IP register is not an actual register; it is simply a circuit that checks for a write operation at the IP address. Any write to that address will cause an initialize operation to take place. The IP register has a standard LSI-11 bus address of 772150. The address selection jumpers on the RQDX2 module determine this address. (See Chapter 3, RQDX2 Configuration, for jumper selection information). The entire initialization sequence can take up to 40 s to complete, 10 s for each of four steps.

When the host Q-Bus processor writes into the IP register, the initialization sequence begins by running the controller self-test diagnostics. If the diagnostics pass, the host enables the next part of the initialization sequence. If the diagnostics fail, the host retries the initialization sequence once more. After a second initialization failure, the system considers the controller inoperable and displays the error code on the controller module.

After successful completion of this portion of the initialization, the host processor uses the SA register.

Status and Address Registers (SA)

The RQDX2 processor and the Q-Bus processor use the SA registers for the MSCP port initialization sequence. The SA register consists of two registers, the SA read register and the SA write register named according to their function in relation to the Q-Bus host processor. Both SA registers occupy the same Q-Bus I/O page address.

The Q-Bus processor writes to the SA write register. The RQDX2's processor reads from the SA write register. The system uses this register during the initialization sequence to pass the MSCP command buffer address and interrupt vector to the RQDX2's processor. The SA register is a standard LSI-11 bus address of 772152. This address is based and dependent on the standard IP address selected using the IP address jumpers.

The RQDX2's processor writes to the SA read register. The Q-Bus reads from the SA read register. The system uses this register to pass initialization status to the Q-Bus processor.

MASS STORAGE CONTROL PROTOCOL (MSCP)

MSCP is the message-oriented set of rules by which the RQDX2 controller module communicates with the host system. MSCP provides the protocol that allows the host to send a command message and the controller module to send a response message. The host designates an area of memory to be used as a communications area and provides the location of this area to the controller module. The size of the communications area is variable and is determined by the host software. Figure 4-1 shows its organization. For additional information regarding MSCP, refer to the UDA50 Programmer's Documentation Kit (QP-905-GZ).

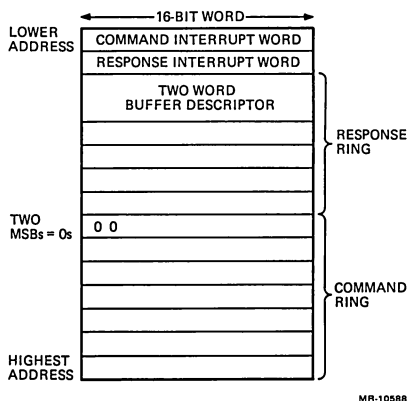


Figure 4-1 Memory Communications Area Organization

MSCP Commands

Table 4-1 lists the MSCP commands and functions supported by the RQDX2 controller module.

Table 4-1 MSCP Commands and Functions

Command	Function
Access	Reads data from the specified unit.
Abort	Guarantees that referenced MSCP command will complete within the controller timeout period.
Available	If specified unit is on-line, returns it to the unit-available state. If specified unit is currently in the unit-available state, this command is essentially a non-operation. (The RQDX2 module cannot spin down a unit.)
Compare Host Data	Reads data from the disk and compares it with the data in the host buffer.
Erase	Writes zeros to the specified logical blocks on the unit. (No data is accessed from the host.)
Get Command Status	Reports on the status of a specified command by returning a number that reflects the command's progress.
Get Unit Status	Reports on the status of a specified unit.
On Line	Places the specified unit on line, if possible.
Read	Reads data starting from the specified logical block on the disk into host memory.
Set Controller Characteristics	Sets host-settable controller characteristics.
Set Unit Characteristics	Sets host-settable unit characteristics.
Write	Writes data starting at the specified logical block on the disk from the host memory.

MSCP Status Codes

The RQDX2 controller module provides MSCP status code response messages. Table 4-2 lists these messages.

Table 4-2 MSCP Status Code Messages

Message	Meaning
Command Aborted	The current command was aborted before it could be completed normally.
Compare Error	While performing a COMPARE command, the system found a discrepancy while comparing the disk data to the host data.
Controller Error	The RQDX2 controller module detected an internal error, but is able to continue processing its outstanding commands.
Data Error	Data could not be read or written due to CRC error "header not found," or due to a sector being read whose forced error bit was set.
Drive Error	The system detected a drive-related error (such as a seek failure).
Media Format Error	The media mounted on the unit was incorrectly formatted.
Host Buffer Access Error	Reports bus timeouts and parity errors during data transfers. (Applies only to the data portion of an MSCP command.)
Invalid Command	The RQDX2 controller module found some field in the command to be in error.
Success	The command was successfully completed.
Unit Available	The RQDX2 controller module is not on-line, but it can accept an On-Line command from the host.
Unit Offline	The RQDX2 controller module is not on-line and cannot be brought on-line.
Write Protected	A write or erase command was attempted to a unit that is either physically or logically write-protected.

DIAGNOSTICS AND UTILITIES PROTOCOL (DUP)

The DUP provides a diagnostic mode of communication between the host Q-Bus processor program and the Diagnostic and Utilities Server Task (DUST). This protocol allows the host program to request that DUST load a diagnostic or utility program and execute it. Some diagnostic programs access the diagnostic blocks on the RD51 disk. This allows the diagnostic to test reading/writing on the disk without accessing or affecting customer software.

During execution of the diagnostic or utility program, the host program can make inquiries to DUST about the progress of the program being executed or abort the program if there are unexpected results.

The diagnostic and utility programs executed by DUP commands (see Table 4-3) may require the host program to specify certain parameters (such as starting host buffer addresses, byte count, block count, and so on). For additional information regarding DUP, see the UDA50 Programmer's Documentation Kit (QP-905-GZ).

Table 4-3 DUP Programs

Program	Function
Write DBN (RD5n only)	Writes and transfers a diagnostic block with a data pattern.
Read DBN (RD5n only)	Reads a diagnostic block.
Format (RD5n only)	Formats the entire disk, verifies the disk, and implements bad block revectoring.
Read Sector (RD5n or RX50)	Reads a physical sector. The data is not transferred to the host, but drive problems will be detected.
Restore (RD5n or RX50)	Moves the read/write head of the drive to the home position.
Self-test	Verifies that certain RQDX2 controller module logic is functioning properly. Self-test results are reported in the diagnostic LEDs (see Chapter 5, Diagnostics). Self-test is always executed on power-up or Bus INIT.

DUP Commands

The RQDX2 controller module supports the following commands which are available to DUP.

- Get DUST Status
- Execute Supplied Program
- Execute Local Program (diagnostic or utility)
- Send Data
- Receive Data
- Abort Program

DUP Responses

The RQDX2 controller module supports the following responses which are available to DUP.

- Success
- Illegal Command

In the case of an Execute Supplied Program command, the following responses are also available.

- No Region Available
- No Region Suitable

In the case of an Execute Local Program command, the following responses are also available.

- No Region Available
- No Region Suitable
- Program Not Known
- Load Failure

INTRODUCTION

There are three diagnostic programs for performing various functional tests on the RQDX2 module. They include the self-test, XXDP+ (PDP-11 systems), and MMS (MicroVAX systems) diagnostics. These diagnostic programs determine whether or not the RQDX2 controller module, the RD5n disk drive(s), and/or the RX50 diskette drive are working properly. If a failure occurs, the diagnostics isolate the faulty component.

XXDP+ and MMS diagnostics are exclusively for maintenance purposes and play no part in normal system operation. The programs are available from Digital Equipment Corporation.

SELF-TEST DIAGNOSTICS

The module executes a self-test diagnostic each time the RQDX2 controller module is powered up or initialized, to verify the operation of the T-11 chip, the ROM and RAM memory chips. Successful completion of the self-test takes a maximum of 10 s. The RQDX2 has a set of four diagnostic LEDs that display a code corresponding to the functional block of the self-test currently being executed or the type of error that has occurred. A description of the LEDs and error codes follows.

Self-test Diagnostic Error LEDs

During the self-test, the diagnostic LEDs mounted on the RQDX2 controller module indicate test errors. On power-up, all of the LEDs turn on and then immediately turn off when the RQDX2 module enters the self-test. The LEDs indicate (in a BCD form) the functional block of the self-test or the type of error that has occurred. Figure 5-1 shows the diagnostic LED locations on the RQDX2 module. Table 5-1 lists the LED error codes and the corresponding error definition.

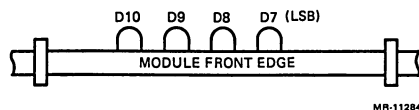


Figure 5-1 Diagnostic LED Locations

Table 5-1 Diagnostic LED Error Displays

LEDs				Error Definition
D10	D9	D8	D7 (LSB)	
On	On	On	On	Beginning power-up testing
Off	Off	Off	On	Performing T-11 processor test
Off	Off	On	Off	Performing T-11 timer/counter/address generator test
Off	Off	On	On	Performing Q22-Bus timer/counter/address generator test
Off	On	Off	Off	Performing Serializer/Deserializer test
Off	On	Off	On	Performing CRC generator test
Off	On	On	Off	Performing hardware version test
Off	On	On	On	Performing ROM checksum test
On	Off	Off	Off	Performing RAM test
On	Off	Off	On	Performing diagnostic interrupt test
On	Off	On	Off	Performing shuffle oscillator test
On	Off	On	On	Performing valid configuration test
On	On	Off	Off	Not used
On	On	Off	On	Not used
On	On	On	Off	Not used
Off	Off	Off	Off	Testing completed

XXDP+ DIAGNOSTICS

The XXDP+ diagnostic system software provides the diagnostic programs necessary to test the RQDX2 controller module, as well as any RD5n disk drive(s) and/or RX50 diskette drive that are connected to the RQDX2 module. Table 5-2 lists the appropriate XXDP+ diagnostic programs and the testing function performed by each program. You can use the individual program listings to further isolate failures.

Table 5-2 XXDP+ Diagnostic Programs

XXDP+ Program Name	Function
ZRQA?? .BIN *	RDRX Performance Exerciser
ZRQB?? .BIN †	RDRX Formatter ††

* ?? Indicates revision of the program (F0 or later).
 † ?? Indicates revision of the program (C1 or later).
 †† This program formats the RD5n disk. The procedure is described in the system technical manuals.

MMS DIAGNOSTICS

The MicroVAX Maintenance System (MMS) diagnostics provide the necessary programs to verify the operation of all MicroVAX system components. Two versions of the MMS diagnostics are available: the customer version that is loaded from a disk that Digital supplies with the system, and the service version that users can purchase separately. Both versions are menu driven allowing the customer to select commands. The customer version supports only the system test and the list and exit commands; the service version supports all the commands.

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Appendix A

RQDX2 Controller Module Backplane Pin Assignments

Digital Equipment Corporation's plug-in modules, including the RQDX2 controller module, all use the same contact (pin) identification system. Figure A-1 shows the contact finger identification for a typical quad-height module. Each connector contains 36 lines (18 lines on each side of the printed circuit board). Table A-1 lists the backplane pin assignments for the RQDX2 controller module.

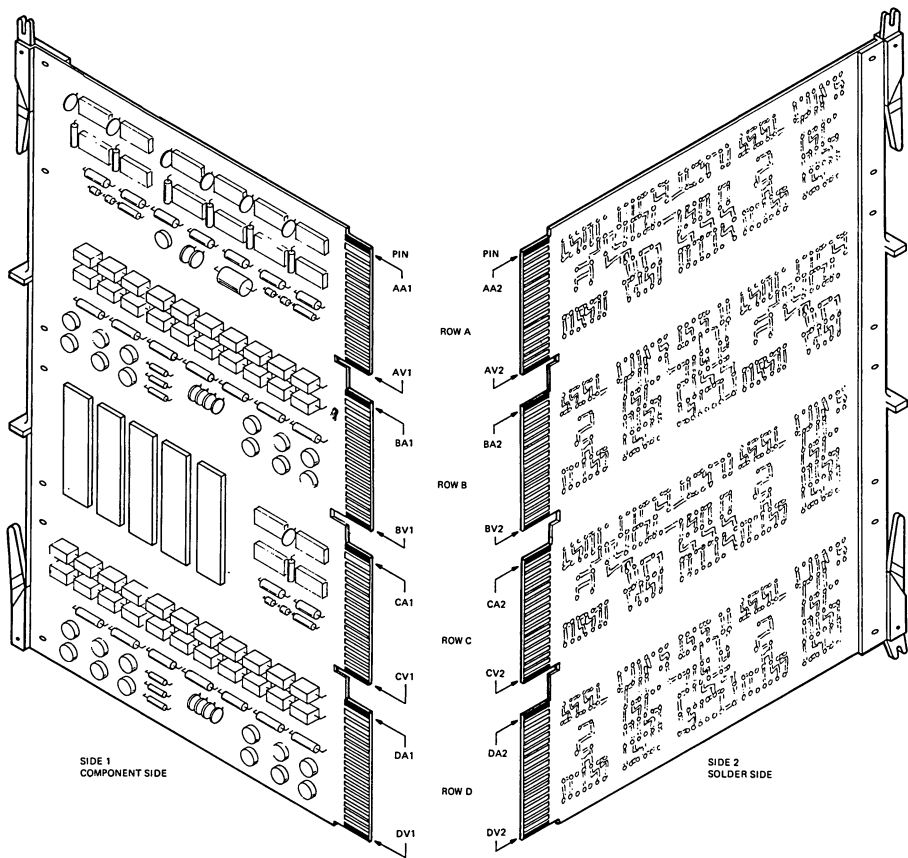


Figure A-1 Quad Module Contact Finger Identification

Table A-1 RQDX2 Controller Module Backplane Pin Assignments

Pin	Signal Name	Pin	Signal Name
AA1	(BIRQ5 L)	AA2	+5 V
AB1	(BIRQ6 L)	AB2	(-12 Vdc)
AC1	BDAL16 L	AC2	GND
AD1	BDAL17 L	AD2	(+12 Vdc)
AE1	(SSPARE1 or +5 B)	AE2	BDOUT L
AF1	(SSPARE2)	AF2	BRPLY L
AH1	(SSPARE3)	AH2	BDIN L
AJ1	GND	AJ2	BSYNC L
AK1	(MSPAREA)	AK2	BWTBT L
AL1	(MSPAREB)	AL2	BIRQ4 L
AM1	GND	AM2	BIAKI L
AN1	BDMR L	AN2	BIAK0 L
AP1	(BHALT L)	AP2	BBS7 L
AR1	BREF L	AR2	BDMGI L
AS1	(+12 B or +5 B)	AS2	BDMG0 L
AT1	GND	AT2	BINIT L
AU1	(PSPARE1)	AU2	BDAL0 L
AV1	(+5 B)	AV2	BDAL1 L
BA1	(BDC0K H)	BA2	+5 Vdc
BB1	BP0K H	BB2	(-12 Vdc)
BC1	BDAL18 L	BC2	GND
BD1	BDAL19 L	BD2	+12 Vdc
BE1	BDAL20 L	BE2	BDAL2 L
BF1	BDAL21 L	BF2	BDAL3 L
BH1	(SSPARE8)	BH2	BDAL4 L
BJ1	GND	BJ2	BDAL5 L
BK1	(MSPAREB)	BK2	BDAL6 L
BL1	(MSPAREB)	BL2	BDAL7 L
BM1	GND	BM2	BDAL8 L
BN1	BSACK L	BN2	BDAL9 L
BP1	(BIRQ7 L)	BP2	BDAL10 L
BR1	(BEVNT L)	BR2	BDAL11 L
BS1	(+12 B)	BS2	BDAL12 L
BT1	GND	BT2	BDAL13 L
BU1	(PSPARE2)	BU2	BDAL14 L
BV1	+5 Vdc	BV2	BDAL15 L
CA1	(Unused)	CA2	+5 Vdc
CB1	(Unused)	CB2	(Unused)
CC1	(Unused)	CC2	GND
CD1	(Unused)	CD2	(Unused)
CE1	(Unused)	CE2	(Unused)
CF1	(Unused)	CF2	(Unused)
CH1	(Unused)	CH2	(Unused)
CJ1	GND	CJ2	(Unused)
CK1	(Unused)	CK2	(Unused)
CL1	(Unused)	CL2	(Unused)
CM1	GND	CM2	CIAKI L

Table A-1 RQDX2 Controller Module Backplane Pin Assignments (Cont.)

Pin	Signal Name	Pin	Signal Name
CN1	(Unused)	CN2	CIAKO L
CP1	(Unused)	CP2	(Unused)
CR1	(Unused)	CR2	CDMGI L
CS1	(Unused)	CS2	CDMGO L
CT1	GND	CT2	(Unused)
CU1	(Unused)	CU2	(Unused)
CV1	(Unused)	CV2	(Unused)
DA1	(Unused)	DA2	+5 Vdc
DB1	(Unused)	DB2	(Unused)
DC1	(Unused)	DC2	GND
DD1	(Unused)	DD2	(Unused)
DE1	(Unused)	DE2	(Unused)
DF1	(Unused)	DF2	(Unused)
DH1	(Unused)	DH2	(Unused)
DJ1	GND	DJ2	(Unused)
DK1	(Unused)	DK2	(Unused)
DL1	(Unused)	DL2	(Unused)
DM1	GND	DM2	(Unused)
DN1	(Unused)	DN2	(Unused)
DP1	(Unused)	DP2	(Unused)
DR1	(Unused)	DR2	(Unused)
DS1	(Unused)	DS2	(Unused)
DT1	GND	DT2	(Unused)
DU1	(Unused)	DU2	(Unused)
DV1	(Unused)	DV2	(Unused)

BLANK

Appendix B
RQDX2 Controller Module Cable Signals

Table B-1 lists the RQDX2 controller module signals on the J1 connector.

Table B-1 J1 Connector Signals

J1 Pin	Signal Name
1	MFMRWRTDT1 (H) (RD5n only signal)
2	MFMRWRTDT1 (L) (RD5n only signal)
3	GROUND
4	HEAD SEL 2 (L) (RD5n only signal)*
5	GROUND
6	SEEKCLPT (L) (RD5n only signal)
7	RD1 RDY (H) (RD5n only signal)
8	WRT FAULT (L)
9	DRVBUSOE (L)
10	HEAD SEL 1 (L) (RD5n only signal)
11	RD2 RDY (H) (RX50 or RD5n)
12	RD0 RDY (H) (RD51 only signal)
13	RD2 WRTPRO (L) (RX50 or RD5n)
14	DRVSLOACK (L) (RD5n only signal)
15	MFMRDDAT0 (H) (RD5n only signal)
16	MFMRDDAT0 (L) (RD5n only signal)
17	MFMRWRTDT0 (H) (RD5n only signal)
18	MFMRWRTDT0 (L) (RD5n only signal)
19	MFMRDDAT1 (H) (RD5n only signal)
20	MFMRDDAT1 (L) (RD5n only signal)
21	GROUND
22	REDUCWRTI (L)
23	RDOWRTPRO (L) (RD5n only signal)
24	DRV SEL 4 (L)
25	GROUND
26	INDEX (L)
27	RD1WRTPRO (L) (RD5n only signal)
28	DRV SEL 1 (L)
29	DRV SEL 2 (L)
30	DRV SEL 3 (L)
31	RD3 RDY (H) (RX50 or RD5n)
32	RXMOTORON (L) (RX50 only signal)
33	GROUND
34	DIRECTION (L)
35	GROUND

* Reserved for future use.

Table B-1 J1 Connector Signals (Cont.)

J1 Pin	Signal Name
36	STEP (L)
37	GROUND
38	RXWRTDATA (L) (RX50 only signal)
39	GROUND
40	WRT GATE (L)
41	GROUND
42	TRACK 00 (L)
43	RD3/WRTPRO (L) (RX50 or RD5n)
44	DRVSLACK (L) (RD5n only signal)
45	GROUND
46	READ DATA (L) (RX50 only signal)
47	GROUND
48	HEAD SEL 0 (L)
49	GROUND
50	READY (L)

Appendix C

Disk Drive Cable Connector Pin Assignments

RD5n DISK DRIVE CONNECTOR PIN ASSIGNMENTS

Tables C-1 through C-3 list the connector pin assignments for the RD5n disk drive signal and power cables.

Table C-1 RD5n Disk Drive J1 Signal Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
1	2	Reserved
3	4	Head Select 2
5	6	Write Gate
7	8	Seek Complete
9	10	Track 0
11	12	Write Fault
13	14	Head Select 0
15	16	Reserved (to J2 pin 7)
17	18	Head Select 1
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Drive Select 4
33	34	Direction In

Table C-2 RD5n Disk Drive J2 Signal Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	Drive Selected
4	3	Reserved
6	5	Reserved
8	7	Reserved (to J1 pin 16)
	9, 10	Reserved
12	11	GND
	13	+MFM Write Data
	14	-MFM Write Data
16	15	GND
	17	+MFM Read Data
	18	-MFM Read Data
20	19	GND

Disk Drive Cable Connector Pin Assignments

Table C-3 RD5n Disk Drive J3 Power Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	+12 V
3	4	+5 V

RX50 DISKETTE DRIVE CONNECTOR PIN ASSIGNMENTS

Tables C-4 and C-5 list the connector pin assignments for the RX50 diskette drive signal and power cables.

Table C-4 RX50 Diskette Drive J1 Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
1	2	TK43L (controls write current level)
3	4	Reserved
5	6	Drive Select 3 L
7	8	Index L
9	10	Drive Select 0 L
11	12	Drive Select 1 L
13	14	Drive Select 2 L
15	16	Motor On L
17	18	Direction (head movement direction)
19	20	Step L (head movement distance)
21	22	Write Data L
23	24	Write Gate L
25	26	Track 0 L
27	28	Write Protect L
29	30	Read Data L
31	32	Reserved
33	34	Ready L

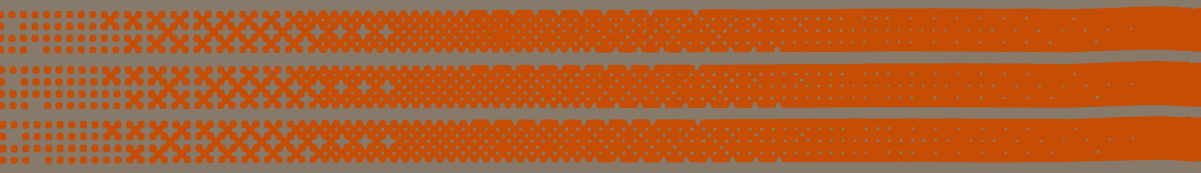
Table C-5 RX50 Diskette Drive J3 Power Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	+12 V
3	4	+5 V

BLANK

BLANK

BLANK



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